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REMARKS

By this Amendment, changes have been made to pages 1, 5 and 6 of the specification. Claims 6 and 10 are cancelled, while claims 4 and 8 are amended. A detailed discussion of these changes follows.

As requested by the Examiner, paragraph [0004] of the published application has been amended to replace the name "Lexington" with the name "Johannessen"; paragraph [0020] has been amended to replace the phrase "Frame 3, 36" with the phrase "Frame C, 36"; and paragraph [0023] has been amended to replace the phrase "represented as load" with the phrase "represented as resistor".

The Examiner objected to the disclosure under 37 CFR 1.71(a), stating that it is not sufficiently enabling. Specifically, the Examiner notes that page 6, lines 15-18 of the disclosure state that a capacitive load can be connected in parallel to the main delay line or one of the smaller delay lines, and that such a configuration will not work properly. This objection is respectfully traversed. The disclosure, at the specified location, does not state that a capacitive load can be connected in **parallel** to the main delay line. In referencing the "capacitive load C" (line 15, page 6), the Applicant is referring specifically to plate 54, which, in respect of the quarter-wave trap 46, forms the capacitor C. (Capacitor C may also act as an antenna, as described on page 6, 4th paragraph). As illustrated by Figure 3, plate 54 is attached to the short-circuited delay-line 28. If the transient behaviour of the delay lines 26 and 28 are ignored, these lines can be approximated as a simple lead having inductance L. Therefore ***L and C are connected in series***. Because C is added to the oscillatory circuit, the frequency of oscillation caused by the delay lines is decreased.

The disclosure has been amended in paragraphs [0024] and [0025] to clarify that the capacitor C is represented by plate 54 in Figure 3 and that the capacitor is connected in series. In addition, claims 4 and 8 are amended to replace the word "parallel" with the phrase "in series". Applicants respectfully submit that these amendments to the disclosure at page 6 and to claims 4 and 8 overcome the Examiner's objection to the drawings under 37 C.F.R. 1.83(a).

Claims 6 and 10 are cancelled, thereby rendering moot, the rejection thereof under 35 U.S.C. 101.

The remaining claims, 1-5 and 7-9, stand rejected under 35 U.S.C. 103(a) as being unpatentable over the following U.S. Patents: U.S. 4,165,482 (Gale); U.S. 4,542,358 (Boby); U.S. 3,631,266 (Kassabgi); U.S. 6,225,864 (Luu); U.S. 3,402,370 (Ross) and U.S. 6,864,760 (Tsuru et al.). Applicants respectfully traverse these rejections in view of the following arguments.

As set forth for example in claim 1, the subject invention is directed to an RF pulse generating device that employs a main delay line, a low impedance electrically driven impulse generator and a quarter-wave trap between the impulse generator and the main delay line. The main delay line is connected to the electrically driven impulse generator at one end and is short-circuited at an opposite end. The output impedance of the impulse generator is selected to be small compared to the characteristic impedance of the main delay line, so that the main delay line becomes an oscillatory circuit. In this manner, the claimed invention uses delay lines to generate high power radio frequency (RF) pulses with high energy content in a single pulse of length between hundreds of nanoseconds to a few microseconds.

The suggestion that the combination of Gale with Boby and Kassabgi renders any of the claims obvious is simply not supported by the teachings of the cited references. Gale is directed

to a method of and apparatus for locating a fault in a conductor. Contrary to the assertions made by the Examiner, Gale nowhere discloses a radio frequency (RF) pulse generator or the use of a delay line in such a generator. The conductor under test in Gale's device clearly has nothing to do with the device itself and certainly cannot be said to be a delay line as that term is used in claim 1 of the subject application. For these reasons alone, the combination of teachings asserted by the Examiner cannot provide a prima facie case of obviousness under 35 U.S.C. 103 of any of the pending claims.

Furthermore, even if the combination of references did establish a prima facie case of obviousness, the combination is nevertheless improper because it clearly relies on the impermissible use of hindsight through reference to Applicant's own disclosure. Absent the use of hindsight, there would be no motivation to combine the various elements from the references in the manner asserted by the Examiner. In particular, no one would be motivated to use the quarter- wave trap of Boby's cable protector in Gale's device for this would defeat the whole purpose of Gale's device, which is to intentionally apply pulses to the conductor under test. Adding the short circuit feature of Kassabgi to the already improper combination of Gale and Boby would further frustrate the purpose of the devices in these references. It is clearly improper to pick and choose elements from a combination of references, each of which discloses an unrelated device, in attempt to establish obviousness of a claimed invention. The asserted combination of teachings of Gale, Boby and Kassabgi, as well the other references relied upon in the rejection of the dependent claims, amounts to such an improper combination.

Applicants do not assert that the various elements of the claimed invention, including the main delay line, the low impedance electrically driven impulse generator and the quarter-wave trap are novel in and of themselves. Rather, it is the synergistic result that is obtained when the

elements are specifically combined in the manner recited in claims 1 and 2, whereby a RF pulse generator is formed that can generate high power radio frequency (RF) pulses with high energy content in a single pulse of length between hundreds of nanoseconds to a few microseconds, that renders the invention patentable and non-obvious over the prior art. For these reasons, Applicants respectfully submit that the prior art rejections are clearly traversed.

In view of the foregoing, Applicants respectfully submit that the all of the pending claims are patentable and allowable and that the application is now in condition for allowance. Accordingly, reconsideration and allowance of the application are respectfully requested.

Respectfully submitted,

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